**Topics**

1. Computer Architecture Basics, Instruction Set Design Principles (Chapter 1 and Appendix A)
   1. Computer Architecture definition, System Design Parameters
   2. Classes of computers
   3. Power and Energy, Cost of IC, wafer, die, yield
   4. RISC vs. CISC
   5. Different types of architectures
   6. Address alignment, Addressing modes
   7. Instruction Encoding (Fixed vs. Variable)
2. Performance Measurement (Chapter 1)
   1. Execution Time & Speedup
   2. Amdahl’s Law
   3. CPI, Bandwidth / Throughput, Latency / Response Time
3. Memory Hierarchy (Chapter 2, Appendix B)
   1. Need for memory hierarchy
   2. Locality principles
   3. Direct, n-way, full-associative cache organizations
   4. Write through, Write back schemes
   5. Cache performance
   6. Basic cache optimizations
   7. Advanced cache optimizations
   8. Virtual Memory
4. Instruction-Level Parallelism, Basic Pipelining (Chapter 3 Secs. 3.1, 3.2, 3.3, Appendix C)
   1. Pipeline diagram, Pipeline performance (ideal speedup)
   2. Pipeline implementation
   3. Structural, Control, and Data hazards (identification and fixing the hazards)
   4. Basic compiler techniques for exposing ILP
   5. Control hazards – static branch prediction, dynamic branch prediction, branch-prediction buffers
5. RISC-V architecture (Section A.9)
   1. Registers, Data Types, Instruction Format
   2. RISC-V Operations
   3. Control-flow instructions, FP instructions
6. Instruction-Level Parallelism (Chapter 3, Secs.3.4, 3.5, 3.6, 3.7, 3.8, 3.11)
   1. Dynamic Scheduling
   2. Tomosulo’s algorithm
   3. Hardware-Based Speculation
   4. Multiple Issue and Static Scheduling, VLIW Approach
   5. Superscalar, Coarse MT, Fine MT, and SMT approaches – basic understanding
7. Data Level Parallelism (Chapter 4, Secs. 4.1, 4.2)
   1. Basic Vector Architecture Idea
   2. RISC64 Vector Architecture
   3. Multiple Lanes, Vector Length Registers, Predicate Registers
   4. Vector Chaining, Strip Mining, Vector Stride, Gather Scatter
8. Thread Level Parallelism (Chapter 5, Secs 5.1, 5.2, 5.4)
   1. Centralized Shared-Memory Architecture
   2. Cache Coherence – Snooping Coherence Protocol
   3. Cache Coherence state diagram (Figure 5.7)
   4. Distributed Shared-Memory Architecture
   5. Directory-Based Cache Coherence Protocol
   6. Directory Based State Transition diagram (Figure 5.20 and 5.21)

**Final Exam Review**

* Wednesday, 30th April
* Review all lecture slides and homeworks
* Review example problems in the textbook
* Solve the sample exam

**Exam Date/Time**

* When: Monday, 5th May 2025
* Time: 3 pm – 5 pm (2 hours)
* Where: Classroom (in person).

**Exam Format**

* Closed notes and closed text.
* You can bring a scientific calculator.
* You are allowed **one** 8.5” x 11” sheet with **hand-written** notes; you can write on both sides.
* **Formula sheet will be provided.**
* **Eight (8) questions will be given on each of the eight topics listed above.**
* You need to answer all the questions. Each question carries 10 pts each.

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